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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Xiujun Guan

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EXAMINER

SURYAWANSHI, SURESH

ART UNIT

PAPER NUMBER

2115

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/735,104

Applicant(s)

GUAN, XIUJUN

Examiner

Suresh K. Suryawanshi

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 May 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/27/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Objections

2. Claim 11 is objected to because of the following informalities: claim 11 is a duplicate claim as claim 6. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Provided Prior Art (APPA) in view of Ning (US Patent 6,477,221).

5. As per claim 1, APPA discloses

a cache capable of storing data [Fig. 1; CACHE];

a control logic capable of controlling a flow of data [Fig. 1; CONTROL LOGIC]; and

at least one core coupled to the cache and the control logic, capable of generating a multiple of CPU clock signal [Fig. 1; CORE] having,

an instruction cache capable of storing data [Fig. 2; INSTRUCTION CACHE];

an instruction fetch unit capable of fetching data [Fig. 2; INSTRUCTION FETCH UNIT];

a plurality of integer execution units coupled to the instruction fetch unit [Fig. 2; IEU].

APPA does not disclose having only one floating-point unit. APPA discloses having plurality of floating point units corresponding to plurality of integer units. However, Ning clearly discloses having only one floating-point unit corresponding to a plurality of integer units [col. 6, lines 30-34]: Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have only one floating-point unit connected to a plurality of integer units. Moreover, as a result of the merging circuits having been constituted in such a configuration, the overall area of the circuit can be reduced, thereby enabling provision of a compact semiconductor chip.

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6. As per claim 12, APPA discloses that the multiple of the CPU clock signal comprises a higher frequency clock having a higher frequency than the CPU clock signal [page 2, lines 1-4].

7. As per claim 13, APPA discloses that the floating-point graphics unit comprises a multiplier pipeline and an adder pipeline [page 2, lines 16-18].

8. Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Provided Prior Art (APPA), Ning (US Patent 6,477,221) and in view of Sung et al (US Patent 6,177,844; hereinafter Sung).

9. As per claim 2, APPA and Ning disclose the invention substantially. APPA and Ning do not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the delay-locked loop circuit comprises of a charge pump circuit [Fig. 2B]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

10. As per claim 3, APPA and Ning disclose the invention substantially. APPA and Ning do not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the delay-locked loop circuit comprises of a voltage controlled delay line [Fig. 2B; col. 5, lines 41-48]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

11. As per claim 4, APPA and Ning disclose the invention substantially. APPA and Ning do not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the delay-locked loop circuit comprises of a control signal capable of controlling the CPU clock signal by propagating through a plurality

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of inverters [Fig. 4B; col. 7, lines 30-33]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

12. As per claim 5, APPA and Ning disclose the invention substantially. APPA and Ning do not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the delay-locked loop circuit comprises of a charge pump circuit [Fig. 2B]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

13. As per claim 6, APPA and Ning disclose the invention substantially. APPA and Ning do not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the delay-locked loop circuit comprises at least one symmetric NOR and one symmetric NAND capable of combination signals [col. 8, lines 50-52]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

14. As per claim 7, APPA and Ning disclose the invention substantially. APPA and Ning do not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the voltage control delay line unit further comprises a delay line unit having at least two inverters [Fig. 4B]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

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combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

15. As per claim 8, APPA and Ning disclose the invention substantially. APPA and Ning do not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the voltage control delay line unit further comprises a delay line unit having at least two inverters [Fig. 4B] and at least two inverters are manipulated into a control signal by a phase frequency detector and the charge pump [Fig. 2B; FEED-BAC IN]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

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16. As per claim 9, APPA and Ning disclose the invention substantially. APPA and Ning do not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that at least two signals are manipulated by the phase frequency [Fig. 2B]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

17. Claim 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Provided Prior Art (APPA), Ning (US Patent 6,477,221), Sung et al (US Patent 6,177,844; hereinafter Sung) and in view of Chung et al (US Patent 6,950,488; hereinafter Chung).

18. As per claim 10, APPA, Ning and Sung disclose the invention substantially. APPA, Ning and Sung do not expressly disclose about a Schmitt circuit. However, Chung clearly discloses using a Schmitt circuit in a delay-locked loop circuit [Fig. 9; col. 3, line 65; col. 8, lines 4-26]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it

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reduces the load of a variable delay unit at high frequency operation and stably locking an external clock signal.

19. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Provided Prior Art (APPA) in view of Sung et al (US Patent 6,177,844; hereinafter Sung).

20. As per claim 14, APPA discloses a circuit comprising a floating point graphics unit [Fig. 2; FGU].

APPA does not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the voltage control delay line unit [Fig. 2B]; a phase frequency detector [Fig. 2B]; a charge pump [Fig. 2B]; at least one symmetric NOR [col. 8, lines 50-52]; at least one symmetric NAND [col. 8, lines 50-52]; and a buffer [Fig. 4B]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits utilizing a delay-locked loop circuitry. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

21. As per claim 15, APPA discloses the invention substantially. APPA and Ning does not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the voltage control delay line unit [Fig. 4B]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

22. As per claim 16, APPA discloses the invention substantially. APPA and Ning does not expressly disclose about a delay-locked loop (DLL) circuit. But a routineer in the art would know that it is well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal. However, Sung clearly discloses about a delay-locked loop circuitry usable in the clock signal distribution networks of programmable logic device integrated circuits [Fig. 2B]. Further, Sung discloses that the voltage control delay line unit further comprises a delay line unit having a plurality of inverters [Fig. 4B]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to integrated circuits functioning as a processor core. Moreover, the improved delay-locked loop circuit will be useful as it more accurately

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emulates the distributed propagation delay of the clock signal being manipulated by the delay-locked loop circuitry.

23. As per claim 17, APPA discloses that a control signal capable of controlling the CPU clock signal is an analog value [Fig. 1 and 2; pages 1-3].

24. As per claim 18, APPA discloses that the multiple of the CPU clock signal is a higher frequency than the CPU clock signal [pages 1-3].

25. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al (US Patent 6,177,844; hereinafter Sung), Applicant Provided Prior Art (APPA) and in view of Ning (US Patent 6,477,221).

26. As per claim 19, Sung discloses

receiving a CPU clock signal [Fig. 2B; CLOCK IN; col. 8, lines 15-22];

delaying the CPU clock signal with at least two inverters [Fig. 2B; voltage controlled delay line; Fig. 4B; inverters; col. 5, lines 41-48; col. 7, lines 30-33];

generating a plurality of output signals [Fig. 2B; col. 4, lines 15-21].

Sung does not disclose about integer units and floating-point units. APPA clearly discloses where a plurality of clock signals pass through a plurality of integer units and then floating-point units [Fig. 1 and 2; pages 1-3]. Sung and APPA do not disclose about combining the plurality of signals from the plurality of output signals to generate a combined custom clock signal. However, Ning clearly discloses having only one floating-point unit corresponding to a plurality of integer units [col. 6, lines 30-34]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have only one floating-point unit connected to a plurality of integer units. Moreover, as a result of the merging circuits having been constituted in such a configuration, the overall area of the circuit can be reduced, thereby enabling provision of a compact semiconductor chip.

27. As per claim 20, Sung and APPA discloses the invention substantially. Sung and APPA do not suggest about producing a control signal with a first signal and a last signal from the plurality of output signals. In other words, combining the plurality of output signals and generating a control signal. However, Ning clearly discloses having only one floating-point unit corresponding to a plurality of integer units [col. 6, lines 30-34]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have only one floating-point unit connected to a plurality of integer units. Moreover, as a result of the merging circuits having been constituted in such a configuration, the overall area of the circuit can be reduced, thereby enabling provision of a compact semiconductor chip.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks

April 27, 2006



**CHUN CAO
PRIMARY EXAMINER**